

2020

COMPUTER SCIENCE — HONOURS

Paper : CC-1

(Digital Logic)

Full Marks : 50

*The figures in the margin indicate full marks.**Candidates are required to give their answers in their own words as far as practicable.*Answer **question no. 1** and **any four** from the rest.

1. Answer **any five** questions from the following : 2×5
- Given $F_1 = \sum m(0, 4, 5, 6)$ and $F_2 = \sum m(0, 3, 6, 7)$. Find the expression $F_1 + F_2$.
 - Realize EX-NOR by NAND gates only.
 - Differentiate between SRAM and DRAM.
 - Perform $(52)_{10} - (62)_{10}$ using 2's complement method.
 - What is biased exponent? What are its advantages?
 - Draw circuit diagram of 2-input TTL NAND gate.
 - What is fan out of a logic gate?
 - A staircase light is controlled by two switches, one at the top and another at the bottom of the stairs. Design a truth table for this system.
2. (a) Realize the following logic expression by NOR gates only $Y = \overline{\overline{\overline{A}BCD}}$. .
- (b) Simplify the following expression and implement it by logic gates.
- $$Y = \sum(1, 3, 7, 11, 15) + d(0, 2, 5, 8, 10)$$
- Draw the truth table.
- (c) What are the maxterms in this expression? 4+5+1
3. (a) Convert $(1231)_4$ into its hexadecimal equivalent.
- (b) Add : $(3D \cdot 2A)_{16} + (4E \cdot 1B)_{16}$
- (c) What are the differences between weighted and non-weighted code?
- (d) What is floating point representation? Why is it required? Give example. 3+2+2+3

Please Turn Over

4. (a) Design Y_{Sum} of a 3-bit full adder by NAND gates only.
(b) Implement Y_{carry} of a 3-bit full adder by 4:1 multiplexers and other basic gates. 4+6
 5. Design an adder by discrete logic gates which can add two numbers A_1A_0 and B_1B_0 . 10
 6. (a) Design a master-slave flip-flop by NAND gates only. Explain its working principle.
(b) What is race around condition? (5+3)+2
 7. (a) Design a decade counter which can count in descending order.
(b) What is negative edge triggered clock? 8+2
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