Mode of Examination: Online
M.Sc.(Computer Science) Semester–I Examination, 2020

2020

Subject: Computer Science

Paper Code & Name: CSM101 (ADVANCES IN COMPUTER ARCHITECTURE)

Full Marks: 70

Date: 16.03.2021 Time and Duration: 12.00 PM – 3:00 PM (3:00 Hours)

Please follow the following instructions carefully:
Promise not to commit any academic dishonesty.
Marks will be deducted if the same/similar answers are found in different answer-scripts.
Candidates are required to answer in their own words as far as applicable.
Each page of the answer scripts should have your University Roll # on the right-top corner.

The name of the scanned copy of the answer script will be of the following format:
(Example: CSM101-ACA-My Roll Number.pdf)
The subject of the mail should be the file name only.
The name of the scanned answer-script is to be sent to cucse2020@gmail.com
The report should have the top page (Page #1) as an index page; mention page number(s) against the answer of each question number.
The answer-script may not be accepted after the scheduled time.

Answer Question #1, Question #2, and any four from the remaining.

1. Answer any 5 (five) questions: [5x2=10]

   a. What are the desirable properties of the RISC architecture?

   b. Critically comment on the phrase - 'execution of instruction'.

   c. How will you justify the usage of cache memory? Express the claim in terms of the relevant parameter set.

   d. What do you mean by 'degree of parallelism'?

   e. What are CPI and MIPS? How are they related?

   f. Discuss the alternative flow control strategies in any message passing system?

   g. 'Pipeline performance increases with the number of stage increases' - Critically comment on the statement.

   h. What is systolization for computer architecture?

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2. Answer any 5 (five) questions: [5x4=20]

   a. What do you mean by mapping a permutation in MICN? Prove that a MICN (NxN) with $\log_2 N$ stages comprising of 2x2 switches cannot be a non-blocking MICN.

   b. Write an algorithm to add 23 numerical values using a static cube connected (N=8) processor setup.

   c. What is the theoretical upper limit of MAL of a static pipeline architecture? Justify the claim.

   d. How is a systolic-array of processors different from SIMD environment? Explain briefly with example.

   e. 'Algorithm depends on underlying processor architecture' – Critically comment on the statement.

f. What are speedup, throughput, and efficiency for a pipelined processor having k number of stages and n number of tasks?

g. What are different types of internal data forwardings? Give examples.

h. Estimate the performance degradation factor in pipelined architecture for branch instructions in terms of relevant parameters.

3. a. For the following reservation table, find the initial collision vector, state diagram, and minimal average latency.

	0	1	2	3	4	5	6	7	8
S1	X								X
S2		X						X	
S3			X				X		
S4				X		X			
S5					X				

How will the performance be changed by inserting one unit of delay in the reservation table?

b. What is the lower bound of minimal average latency corresponding to any given reservation table of static pipeline architecture? Justify the answer.

. [7+3]

4. a. Describe in brief various pipeline hazards with at least one solution to each hazard.

b. Discuss with examples 'Write Through' and 'Write Once' protocols for cache consistency.

c. What is Systolic architecture (SA)? Explain the operation of a matrix multiplier SA with a suitable diagram and schedule of data.

[2+3+5]

5. a. Write an algorithm to test whether two input-output pairs of desired connection in a 3-stage Shuffle- Exchange-MICN (8x8) will lead to conflicts or not.

b. Critically comment on XOR and destination tag routing schemes for MICN.

c. Let A be a 2^k x 2^k matrix stored in row-major order in the main memory. Prove that the transposed matrix A^T can be obtained by performing k perfect shuffles on A.

[5+2+3]

6. a. Briefly explain the addressing techniques of cache memories with suitable examples.

b. What is meant by cache-coherency?

c. Briefly explain the alternative techniques to reduce cache miss

[4+2+4]

7. a. With suitable examples, compare loosely-coupled and tightly-coupled system structures.

b. Explain how parallel vector addition can be done in a SIMD computer system.

[5 + 5]

8. a. With a suitable diagram of the Memory Management Unit (MMU) explain the function of the segmentation with a paging-based virtual memory system.

   b. State the difference between paging and segmentation.

   c. What is TLB? Explain the use of TLB.

[5 + 2 + 3]